

Search Report

EIC 2800

STIC Database Tracking Number: 258994

To: STEVEN FULK
Location: JEF-6A81
Art Unit: 2891
Wednesday, April 30, 2008

Case Serial Number: 10/817623

From: DIANE JACKSON
Location: EIC2800
JEF-4B68 / JEF-4B68
Phone: (571)272-3260

diane.jackson@uspto.gov

Search Notes

Attached are litigation search results in Lexis Nexis, and CourtLink and Questel-Orbit.

No Litigation was found for Serial Number 10/817623 .

If you have any questions, please feel free to contact me.

Thanks,

Diane



Selected file: PLUSPAT

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Abstracts/Titles in English , French & German. Increased
standardization
of Assignee/Inventor names. Added cited ref's BE , CH , NL , TR , AU ,
& JPB
For PlusPat Fact Sheet , Pricing and FAQ , see the Questel website
Last update of file: 2008/04/25 (YYYY/MM/DD) 2008-17/UP (last update)

Search statement 2

nbr /pn us6346464

PLUSPAT1 US6346460	1
PLUSPAT2 US6346461	1
PLUSPAT3 US6346462	1
PLUSPAT4 US6346463	1
PLUSPAT5 US6346464	1
PLUSPAT6 US6346465	1
PLUSPAT7 US6346466	1
PLUSPAT8 US6346467	1
PLUSPAT9 US6346468	1
PLUSPAT10US6346469	1
PLUSPAT11US634647	1
PLUSPAT12US6346470	1
PLUSPAT13US6346471	1
PLUSPAT14US6346472	1
PLUSPAT15US6346473	1

Some: numbers / Continue: Y / None: N

Search 2 - 5 - 1

** SS 2: Results 1

Continue: Y / N

prt full legalall max

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US6346464 (B1) Manufacturing method of semiconductor device
PN US6346464 B1 20020212 [US6346464]
TI (B1) Manufacturing method of semiconductor device
PA (B1) TOKYO SHIBAURA ELECTRIC CO (JP)
PA0 Kabushiki Kaisha Toshiba, Kawasaki [JP]
IN (B1) TAKEDA TORU (JP); TSUNODA TETSUJIRO (JP)
AP US60410000 20000627 [2000US-0604100]
PR JP18168799 19990628 [1999JP-0181687]
IC (B1) H01L-021/425
H01L-021/265 [2006-01 A F I R M JP]
H01L-021/261 [2006-01 A - I R M EP]
ICAA H01L-021/266 [2006-01 A - I R M EP]
H01L-029/06 [2006-01 A - I R M EP]
H01L-029/78 [2006-01 A - I R M EP]
H01L-021/02 [2006 C - I R M EP]
ICCA H01L-029/02 [2006 C - I R M EP]
H01L-029/66 [2006 C - I R M EP]
H01L-021/261
EC H01L-021/266
H01L-029/06B2B3R2
H01L-029/78B2
PCL ORIGINAL (O) : 438514000; CROSS-REFERENCE (X) : 257E21330
257E21346 257E29257 438184000 438228000 438268000 438451000
DT Basic
Cited in the search report
-US4472871(A)[US4472871]
CT -US6103578(A)[US6103578]
-EP1003272(A2)[EP1003272]
Cited by the applicant
-US5438215(A)[US5438215]
STG (B1) U.S. Patent (no pre-grant pub.) after Jan. 2, 2001
A method of manufacturing a low power dissipation semiconductor power device is provided which is easy to perform and suitable for mass production. When a first and second conductivity-type regions are formed on a semiconductor substrate which is selectively irradiated by impurity ions, an excellent super junction is formed by controlling the ion acceleration energy and the width of each irradiated region so that the first and second conductivity-type regions may have a uniform impurity distribution and a uniform width along the direction of irradiation. Another method of manufacturing a low power dissipation semiconductor power device having an excellent super junction is provided which selectively irradiates a collimated neutron beam onto a P+ silicon ingot and forms an N+ region that has a uniform impurity distribution and a uniform width along the direction
AB

of irradiation in the P+ silicon ingot.
UP 2002-08

1 / 1 LGST - Legal 
Status - ©EPO

US6346464 20001117 US/ASAASSIGNMENTOWNER: KABUSHIKI KAISHA
TOSHIBA 72 HORIKAWA-CHO, SA...
PN US6346464 B1 20020212 [US6346464]
AP US60410000 20000627 [2000US-0604100]
20001117 US/AS-A
ASSIGNMENT
OWNER: KABUSHIKI KAISHA TOSHIBA 72 HORIKAWA-CHO,
SAIWA-K
ACT ASSIGNMENT OF ASSIGNORS INTEREST;ASSIGNORS:TAKEDA,
TORU;TSUNODA, TETSUJIRO;REEL/FRAME:011311/0492;SIGNING
DATES FROM 20001004 TO 20001005
20040810 US/RF-A
REISSUE APPLICATION FILED
EFFECTIVE DATE: 20040405
UP 2004-34

1 / 1 CRXX - US Claims
Reassignments - ©CLAIMS/RRX

US6346464 20040405 REISSUE REQUESTEDISSUE DATE OF O.G.:
20040810REISSUE REQUEST NUMBER...
AN 3637331
PN 6,346,464 A 20020212 [US6346464]
PA Toshiba Corp JP
PT C (Chemical)
20040405 REISSUE REQUESTED
ISSUE DATE OF O.G.: 20040810
ACT REISSUE REQUEST NUMBER: 10/817623
EXAMINATION GROUP RESPONSIBLE FOR REISSUEPROCESS: 2812

Reissue Patent Number:

UP 2004-33
UACT 2004-08-10

Selected file: FAMPAT

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Abstracts/Titles in English , French & German. Increased standardization
of Assignee/Inventor names. Added cited ref's BE , CH , NL , TR , AU , & JPB
For more details , see the FamPat Fact Sheet and Questel website
Last update of file: 2008/04/25 (YYYY/MM/DD) 2008-17/UP (last update)

Search statement 1

nbr /pn us6346464

FAMPAT1 US6346460	1
FAMPAT2 US6346461	1
FAMPAT3 US6346462	1
FAMPAT4 US6346463	1
FAMPAT5 US6346464	1
FAMPAT6 US6346465	1
FAMPAT7 US6346466	1
FAMPAT8 US6346467	1
FAMPAT9 US6346468	1
FAMPAT10US6346469	1
FAMPAT11US634647	1
FAMPAT12US6346470	1
FAMPAT13US6346471	1
FAMPAT14US6346472	1
FAMPAT15US6346473	1

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Search 1 - 5 - 1

** SS 1: Results 1

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1 / 1 FAMPAT - Patent 
Families - ©Questel

JP2001015448 Manufacturing method of semiconductor device

FAN 20042792240325

PN JP2001015448 A 20010119 [JP2001015448]

PN US6346464 B1 20020212 [US6346464]
JP3851744 B2 20061129 [JP3851744]

TI Manufacturing method of semiconductor device

PA TOKYO SHIBAURA ELECTRIC CO

PA0 Kabushiki Kaisha Toshiba, Kawasaki [JP]

IN TAKEDA TORU; TSUNODA TETSUJIRO

AP 1999JP-0181687 19990628

AP 2000US-0604100 20000627

PR 1999JP-0181687 19990628

H01L-021/02

H01L-021/261

H01L-021/265

H01L-021/266

IC H01L-021/425

H01L-029/02

H01L-029/06

H01L-029/66

H01L-029/78

H01L-021/265 [2006-01 A F I R M JP]

H01L-021/261 [2006-01 A - I R M EP]

ICAA H01L-021/266 [2006-01 A - I R M EP]

H01L-029/06 [2006-01 A - I R M EP]

H01L-029/78 [2006-01 A - I R M EP]

H01L-021/02 [2006 C - I R M EP]

ICCA H01L-029/02 [2006 C - I R M EP]

H01L-029/66 [2006 C - I R M EP]

H01L-021/261

H01L-021/266

EC H01L-029/06B2B3R2

H01L-029/78B2

PCL ORIGINAL (O) : 438514000; CROSS-REFERENCE (X) : 257E21330
257E21346 257E29257 438184000 438228000 438268000 438451000

FI H01L21/265 F; H01L21/26 N; H01L21/265 M
(US6346464)

CT Cited in the search report

-US4472871(A)[US4472871]
-US6103578(A)[US6103578]
-EP1003272(A2)[EP1003272]

Cited by the applicant

-US5438215(A)[US5438215]
(JP2001015448)

(A)

CT [19] Citation as reason for refusal of an application

- JP (A) 2000208527 [JP2000208527]
- JP (A) 1981069823 [JP56069823]
- JP (A) 1998223896 [JP10223896]
(US6346464)

A method of manufacturing a low power dissipation semiconductor power device is provided which is easy to perform and suitable for mass production. When a first and second conductivity-type regions are formed on a semiconductor substrate which is selectively irradiated by impurity ions, an excellent super junction is formed by controlling the ion acceleration energy and the width of each irradiated region so that the first and second

AB conductivity-type regions may have a uniform impurity distribution and a uniform width along the direction of irradiation. Another method of manufacturing a low power dissipation semiconductor power device having an excellent super junction is provided which selectively irradiates a collimated neutron beam onto a P+ silicon ingot and forms an N+ region that has a uniform impurity distribution and a uniform width along the direction of irradiation in the P+ silicon ingot.

OBJ

uniform along the direction of irradiation.

The present invention is a semiconductor device manufacturing method of forming a first and second conductivity-type regions by irradiating impurity ions selectively onto a semiconductor substrate; wherein two shielding masks in a reversed imaging relation to each other are used to restrict the impurity ion irradiated regions so that the cross-sectional shape and the cross-section area of the first and second conductivity-type regions on planes vertical to the irradiation direction may be uniform in the direction of irradiation; and the impurity ion acceleration energy is controlled to make the impurity concentration in the first and second conductivity-type regions uniform in the direction of irradiation.

The present invention is a semiconductor device manufacturing method of forming an N⁺ region by selectively irradiating a neutron beam onto a P⁺ semiconductor ingot, wherein the incident angle of the neutron beam is collimated so that the cross-sectional shape and the cross-section area of the N⁺ region may be uniform in the direction of irradiation and so that the impurity concentration in the N⁺ region may be uniform in the direction of irradiation.

(US6346464)

The present invention has been made to solve the above problem and its principal object is to provide a method of manufacturing low power dissipation semiconductor power devices having the super junction structure. The present invention allows the use of semiconductor ingots made of group IV elements such as germanium and silicon carbide.

Specifically, the ion implantation and the neutron beam irradiation have the following advantages:

ADB (1) Since a selective irradiation can be performed by an electric or magnetic sweep or movement of silicon substrate, the width of irradiation pattern can be continuously controlled according to changes in ion acceleration energy, and the vertical distribution of implanted ions shows an excellent uniformity. A shortcoming in the above prior art is that such manufacturing method of repeating the epitaxial growth process to create low power dissipation semiconductor power devices is costly, difficult to implement and not suitable for mass production.

As described above, by the method of forming a super junction according to the present invention, which does not use conventional complex processes like the epitaxial growth but use only efficient processes such as ion implantation and neutron beam irradiation, a super junction can be formed that has an arbitrary and uniform cross-section in the vertical direction.

(US6346464)

ICLM 1. A semiconductor device manufacturing method of forming a second conductivity-type region by irradiating impurity ions onto a first conductivity-type semiconductor substrate; wherein the impurity ion irradiated region is restricted by a shield mask intercepting said impurity ions and the impurity ion acceleration energy is controlled to provide a uniform impurity distribution in the direction of

irradiation in said second conductivity-type region.

2. A semiconductor device manufacturing method of forming at least one of a first and second conductivity-type regions in a semiconductor substrate by selectively irradiating impurity ions onto said semiconductor substrate; wherein the impurity distributions in said first and second conductivity-type regions are uniform in the direction of irradiation, and the impurity ion acceleration energy and the area of each region irradiated by said impurity ions are controlled so that the cross-sectional shape and cross-section area of said first and second conductivity-type regions on planes perpendicular to the direction of irradiation may be uniform in the direction of irradiation.

12. A semiconductor device manufacturing method of forming a first conductivity-type region and a second conductivity-type region on a semiconductor substrate by irradiating impurity ions onto said semiconductor substrate;

wherein the regions irradiated by impurity ions are restricted by impurity ion intercepting shield masks which are in an inverted imaging relation to each other so that the cross-sectional shape and the cross-section area of the first and second conductivity-type regions on planes perpendicular to the direction of irradiation may be uniform along the direction of irradiation, and the impurity ion acceleration energy is controlled to make the impurity ion distributions in the first and second conductivity-type regions uniform along the direction of irradiation.

14. A semiconductor device manufacturing method of forming an N+ region by irradiating a neutron beam onto a semiconductor ingot having a P+ region;

wherein the incident direction of said neutron beam is collimated to make the cross-sectional shape and the cross-section area of said N+ region on planes perpendicular to the direction of irradiation uniform along the direction of irradiation, and the impurity distribution in said N+ region is controlled to be uniform along the direction of irradiation.

UP 2002-08

1 / 1 LGST - Legal 
Status - ©EPO

US6346464 20001117 US/ASAASSIGNMENTOWNER: KABUSHIKI KAISHA
TOSHIBA 72 HORIKAWA-CHO, SA...

PN US6346464 B1 20020212 [US6346464]

AP US60410000 20000627 [2000US-0604100]
20001117 US/AS-A

ACT ASSIGNMENT
OWNER: KABUSHIKI KAISHA TOSHIBA 72 HORIKAWA-CHO,
SAIWAI-K

ASSIGNMENT OF ASSIGNORS INTEREST;ASSIGNORS:TAKEDA,
TORU;TSUNODA, TETSUJIRO;REEL/FRAME:011311/0492;SIGNING
DATES FROM 20001004 TO 20001005
20040810 US/RF-A
REISSUE APPLICATION FILED
EFFECTIVE DATE: 20040405

UP 2004-34

1 / 1 CRXX - US Claims
Reassignments - ©CLAIMS/RRX

US6346464 20040405 REISSUE REQUESTED ISSUE DATE OF O.G.:
20040810 REISSUE REQUEST NUMBER...
AN 3637331
PN 6,346,464 A 20020212 [US6346464]
PA Toshiba Corp JP
PT C (Chemical)
20040405 REISSUE REQUESTED
ISSUE DATE OF O.G.: 20040810
REISSUE REQUEST NUMBER: 10/817623
ACT EXAMINATION GROUP RESPONSIBLE FOR REISSUEPROCESS: 2812

Reissue Patent Number:

UP 2004-33
UACT 2004-08-10

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Patent Search 6346464 4/30/2008

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Source: Combined Source Set 10 - Utility, Design and Plant Patents

Terms: patno=6346464 ([Edit Search](#) | [Suggest Terms for My Search](#))

604100 (09) 6346464 February 12, 2002

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

6346464

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February 12, 2002

Manufacturing method of semiconductor device

REISSUE: April 5, 2004 - Reissue Application filed Ex. Gp.: 2812; Re. S.N. 10/817,623 (O.G. August 10, 2004)**INVENTOR:** Takeda, Toru - Kokubunji, Japan (JP); Tsunoda, Tetsujiro - Urawa, Japan (JP)**APPL-NO:** 604100 (09)**FILED-DATE:** June 27, 2000**GRANTED-DATE:** February 12, 2002**PRIORITY:** June 28, 1999 - 11181687, Japan (JP)**ASSIGNEE-PRE-ISSUE:** November 17, 2000 - ASSIGNMENT OF ASSIGNEES INTEREST (SEE DOCUMENT FOR DETAILS)., KABUSHIKI KAISHA TOSHIBA 72 HORIKAWA-CHO, SAIWAI-KUKAWASAKI-SHI, (1), Reel and Frame Number: 011311/0492**ASSIGNEE-AT-ISSUE:** Kabushiki Kaisha Toshiba, Kawasaki, Japan (JP), Foreign company or corporation (03)**LEGAL-REP:** Oblon, Spivak, McClelland, Maier & Neustadt, P.C.**PUB-TYPE:** February 12, 2002 - Utility Patent having no previously published pre-grant publication (B1)**PUB-COUNTRY:** United States (US)**US-MAIN-CL:** 438#514**US-ADDL-CL:** 257#E21.33, 257#E21.346, 257#E29.257, 438#184, 438#228, 438#268, 438#451**CL:** 438, 257**SEARCH-FLD:** 438#514, 438#268, 438#184, 438#270, 438#299, 438#302, 438#303, 438#305,

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pre/N	precedes by N words
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w/seg	in same segment
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and not	and not

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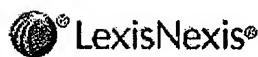
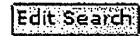
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<u>or</u>	or
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<u>pre/N</u>	precedes by N words
<u>w/p</u>	in same paragraph
<u>w/seg</u>	in same segment
<u>w/s</u>	in same sentence
<u>and not</u>	and not

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(Rule 8.3 of the City Code on Takeovers and Mergers)**1. KEY INFORMATION**Name of person dealing BARCLAYS PLC

(Note 1)

Company dealt in SAINSBURY(J)

Class of relevant security ORD GBP0.28571428

to which the dealings being

disclosed relate (Note 2)

Date of dealing 17 August 2007

2. INTERESTS, SHORT POSITIONS AND RIGHTS TO SUBSCRIBE

(a) Interests and short positions (following dealing) in the class of relevant securities dealt in (Note 3)

Long Short

	Number	(%)	Number	(%)
(1) Relevant	62,693,536	3.60%	2,296,378	0.13%

securities

(2) Derivatives **6,346,464** 0.36% **6,846,869** 0.39%

(other than options)

(3) Options and 2,750 0.00% 0 0.00%

agreements to purchase/sell

Total 69,042,750 3.96% 9,143,247 0.52%

(b) Interests and short positions in relevant securities of the company, other than the class dealt in (Note 3)

Class of Long Short

relevant

security:

Number (%). Number (%)

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